Amendments to Specification

Page 2, rewrite the paragraph starting at line 3, to read as follows:

One of known, conventional image display devices is a liquid crystal display device of an active matrix drive type. The liquid crystal display device, ~~is,~~ as shown in Figure 132, is composed of a pixel array ARY, a scan signal line drive circuit GD, and a data signal line drive circuit SD. The pixel array ARY includes large numbers of scan signal lines GL and data signal lines SL crossing each other. A pixel PIX is provided in each segment that is surrounded by two adjacent scan signal lines GL and two adjacent data signal lines SL, forming a matrix of pixels as a whole. The data signal line drive circuit SD samples an input video signal DAT according to a timing signal, such as a clock signal SCK, amplifies the sampled data as required, and writes the data to associated data signal lines SL. The scan signal line drive circuit GD selects the scan signal lines GL sequentially according to a timing signal, such as a clock signal GCK, and controls opening/closure of those switching elements in the pixels PIX, to write to the pixels PIX the video signal (data) written to the data signal lines SL and also to cause the data written in the pixels PIX to be held.

Pages 62-63, rewrite the paragraph starting at line 20 on page 62, to read as follows:

In Figure 59, first, the digital video signal DIG is latched by the latch circuit LAT and then decoded by a multiplexer MUX. As this happens, a corresponding reference signal is selected from for video signal reference potentials VREF by the reference voltage selection circuit VSEL. Here, if there are relatively many display halftones, the selection switch SWT is switched to intermediate potential generation circuit DAC by the display format control signal FMT, two reference signals

are selected according to higher order bits as an input to the intermediate potential generation circuit DAC and an intermediate potential is produced according to lower order bits. Conversely, if there are relatively ~~a~~ few display halftones, the intermediate potential generation circuit DAC is isolated from the rest, and only one reference signal is selected from for-video-signal reference potentials VREF according to the reference voltage selection circuit VSEL as a direct output to the data signal line SL.